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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Levy et al. Attorney Docket No.: NOVLP063

Patent: 7,005,372 B2 Issued: February 28, 2006

Title: DEPOSITION OF TUNGSTEN NITRIDE

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on August 24, 2006 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Aurelia M. Sanchez

REQUEST FOR CERTIFICATE OF CORRECTION OF OFFICE MISTAKE (35 U.S.C. §254, 37 CFR §1.322)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Attn: Certificate of Correction

Dear Sir:

Attached is Form PTO-1050 (Certificate of Correction) at least one copy of which is suitable for printing. The errors together with the exact page and line number where the errors are shown correctly in the application file are as follows:

SPECIFICATION:

1. Column 2, line 3, change "modem semiconductor" to --modern semiconductor--. This appears correctly in the patent application as filed on October 20, 2003, on page 2, line 18.

2. Column 15, line 32, change "Modem semiconductor" to --Modern semiconductor--. This appears correctly in the patent application as filed on October 20, 2003, on page 21,line 16.

3. Column 17, line 17, change "modem semiconductor" to --modern semiconductor--. This appears correctly in the patent application as filed on October 20, 2003, on page 24, line 8.

CLAIMS:

1. In line 7 of claim 29, (column 24, line 39) insert --wherein-- after "precursor". This appears correctly in the Response to Office Action as filed on June 16, 2005, on page 4, claim 28, line 7.

Patentee hereby requests expedited issuance of the Certificate of Correction because the error lies with the Office and because the error is clearly disclosed in the records of the Office. As required for expedited issuance, enclosed is documentation that unequivocally supports the patentee's assertion without needing reference to the patent file wrapper.

It is noted that the above-identified errors were printing errors that apparently occurred during the printing process. Accordingly, it is believed that no fees are due in connection with the filing of this Request for Certificate of Correction. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. NOVLP063).

Respectfully submitted,
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conformal coverage, chemical vapor deposition (CVD) methods are typically considered. A conventional CVD process involves the simultaneous introduction of gas phase reactants, including tungsten precursor (typically tungsten hexafluoride (WF_6)) and a nitrogen containing gas (e.g., N_2), near a heated wafer surface while a vacuum is applied to the system. The reaction is driven by the energy provided by the heated wafer and the free energy change of the chemical reaction. The growth of the tungsten nitride film continues as long as the reactants and energy source are available.

Although standard tungsten nitride CVD techniques can provide good step coverage and adequately fill low aspect ratio features (e.g., < 5:1 aspect ratio), as semiconductor fabrication technology approaches the nanometer scale, the demands for step coverage and gap filling are becoming more stringent and CVD may not be suitable for the task. Traditional plasma-enhanced CVD of tungsten nitride has relatively poor step coverage for a CVD process (<50% SC in a 5:1 aspect ratio cylindrical contact). This is not adequate for the demands of current and future semiconductor technology with aspect ratios exceeding 10 to 1 and critical dimensions less than 100 nanometers. CVD and particularly PNL or ALD tungsten processes (as opposed to tungsten nitride processes) can provide the very high step coverage and conformal deposition required for modern semiconductor devices, but will not adhere directly to dielectric surfaces. Tungsten now requires an adhesion layer such as TiN before deposition on dielectric surfaces. Finally, the high deposition temperatures required by many TiN deposition techniques (e.g. PECVD-TiN from $TiCl_4$) require high deposition temperatures that are incompatible with low-K dielectrics or nickel silicide.

What are therefore needed are improved methods for depositing tungsten nitride.

SUMMARY OF THE INVENTION

The present invention provides methods for depositing a tungsten nitride layer on a substrate, where the methods provide good tungsten nitride adhesion to the substrate, fine control over deposition thickness, and good step coverage over high aspect ratio regions of the substrate. To accomplish this, the invention provides a pulsed nucleation layer method for depositing tungsten nitride. Generally, the invention employs at least the following operations (performed in various orders): (i) providing a layer of reducing agent on a substrate surface, (ii) contacting the substrate surface with a tungsten containing precursor to form a tungsten layer on the substrate, and (iii) nitriding the tungsten layer to form tungsten nitride.

available for deposition of low resistivity tungsten rather than higher resistivity Ti and TiN.

To recap, some advantages of the tungsten nitride plugfill integration scheme over the traditional Ti-TiN integration scheme are as follows:

1) The ability of the PNL-WN / PNL-W processes to fill contacts and vias with aspect ratios greater than 20:1. This is a significant advance over traditional CVD-TiN and PVD-Ti step coverage performance

2) Elimination of Ti-TiN deposition equipment and processing steps. This simplification will substantially reduce the manufacturing cost of the tungsten plugfill process. In a preferred implementation wafer preclean, PNL-WN, PNL-W, and CVD-W are all completed in a single wafer pass through an integrated cluster tool. This saves on wafer moves from tool to tool, semiconductor cleanroom floor space requirements, and semiconductor manufacturing capital equipment cost by eliminating the Ti-TiN deposition tool.

3) Reduction in semiconductor wafer maximum processing temperature requirements. Modern semiconductor wafer processing thermal budget requirements call for maximum processing temperatures < 450C for contact metallization and <350C for vias in low-K dielectrics. PNL-WN and PNL-W are both typically deposited with wafer temperatures <300C in the preferred implementation.

4) Reduction in post-CMP center seam opening (or coring) of tungsten plugs. As tungsten grows from the sides of a contact or via to the center, a thin seam is typically left at the centerline of the plug. In the case of a Ti-TiN liner barrier stack, the relatively poor step coverage of (PVD) Ti and (CVD) TiN result in an overhang feature at the mouth of the contact. This can result in a feature with a smaller diameter at the top than in the mid-section of the plug. Such an overhang inevitably produces an open seam inside the plug because the growing tungsten film seals the top of the feature before the midsection of the feature is completely filled. Such seams can be exposed during CMP and result in wafer defects. In the case of a PNL-WN / PNL-W liner-barrier film stack, both materials have virtually 100% step coverage and can be deposited very thinly (<50 Angstroms), which results in no overhang and no resulting seam during CVD plugfill.

5) By reducing the total thickness of the liner barrier layer from, say, 200 Angstroms for a typical Ti-TiN implementation to <50Angstroms for PNL-WN (in the preferred

2) PNL-W / PNL-WN / PNL-W / CVD-W

3) PNL WN - CVD-W plugfill

4) WN-W integrated with degas, preclean (DFE or reactive clean)

The capacitors may be trench capacitors, fin capacitors, plate capacitors or any other structure suitable for IC applications. In the case of stacked capacitors the bottom electrode may be deposited on a polysilicon bottom electrode to facilitate structure formation. The extremely high step coverage of PNL-WN and PNL-W are enabling features required for implementation of PNL-WN for modern semiconductor memory cell electrodes.

APPLICATION 4: GATE ELECTRODE

In this application, tungsten nitride functions as an adhesion layer, barrier layer, or primary conductor in a gate electrode. Tungsten nitride may be applied directly on the gate dielectric or on a polysilicon electrode to reduce polysilicon line thickness requirements.

Some of requirements for a transistor gate application include a tunable work function, thermal stability, and resistance to oxidation. Modifying the W/N stoichiometry of the as-deposited film, or adding dopants such as boron (from diborane for example), silicon (from silane for example) and/or nitrogen (from ammonia for example) can tune the work function of PNL tungsten nitride. In addition to boron and nitrogen, typical III-V dopant materials such as Al, Ga, P, and As may also be employed. Another effective way to modulate the work function of PNL-WN is to generate a layered structure of PNL-WN and PNL-W. The number, thickness, and sequence of the layers can be varied, but the preferred implementation is for very thin (< 10Å) layers of alternating PNL-W and PNL-WN, beginning and ending with PNL-W.

As a gate electrode, a PNL tungsten nitride or a tungsten-nitride / tungsten film stack provides a metal gate that resists the charge depletion phenomenon commonly observed in non-metallic gate electrodes such as those fabricated from polysilicon. Charge depletion effectively increases the gate dielectric thickness. A tungsten-nitride / tungsten gate electrode may also be formed on top of a polysilicon gate electrode to reduce the height requirement of the polysilicon gate without changing the gate dielectric / polysilicon interface.

23. (Withdrawn) The method of claim 1, further comprising forming a metallic tungsten layer on the tungsten nitride layer to form a gate electrode comprised of the tungsten nitride layer together with the metallic tungsten layer.

24. (Withdrawn) The method of claim 1, further comprising forming a metallic tungsten layer on the tungsten nitride layer to form a capacitor electrode comprised of the tungsten nitride layer together with the metallic tungsten layer.

25. (Original) The method of claim 1, further comprising forming a metallic tungsten plug on the tungsten nitride layer to form a tungsten interconnect, wherein the tungsten nitride layer serves as at least one of an adhesion layer, a diffusion barrier layer, and a nucleation layer for subsequent tungsten deposition.

26. (Original) The method of claim 25, further comprising depositing a titanium layer prior to formation of the tungsten nitride layer.

27. (Original) The method of claim 1, wherein each of the boron-containing agent, the tungsten-containing precursor, and the nitriding agent are delivered in an inert carrier gas or in a mixture of inert gas with N_2 or H_2.

28. (Currently Amended) A method of forming a tungsten nitride layer on a substrate, the method comprising:

(a) positioning the substrate in a deposition chamber;

(b) ~~depositing~~ exposing the substrate to a gas phase reducing agent ~~onto the substrate to form a layer of reducing agent on the substrate~~;

(c) exposing the ~~layer of reducing agent~~ substrate to a tungsten containing precursor ~~to form a tungsten layer~~, wherein (b) and (c) are performed sequentially in any order and together form a tungsten layer;

(d) exposing the tungsten layer to a nitriding agent to form a first portion of the tungsten nitride layer; and

(e) repeating (b) through (d) for one or more cycles to complete formation of the tungsten nitride layer;

wherein one or more of the reducing agent, the tungsten containing precursor, and the nitriding agent comprise a different compound when employed to form the first portion of the tungsten nitride layer and when employed in (e).

29. (Original) The method of claim 28, wherein the reducing agent is a borane.

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Approved for use through 6/30/99. OMB 0651-0033
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PT-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,005,372 B2 Page 1 of 1

DATED : February 28, 2006

INVENTOR(S) : Levy et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

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Column 2, line 3, change "modem semiconductor" to --modern semiconductor--.

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In the Claims:

In line 7 of claim 29, (column 24, line 39) insert --wherein-- after "precursor".

MAILING ADDRESS OF SENDER:

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